VE-HEP: **H**ardening the value chain through open source, trustworthy **E**DA tools and **P**rocessors

Towards a Free and Open EDA Supply Chain

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An Open Toolchain

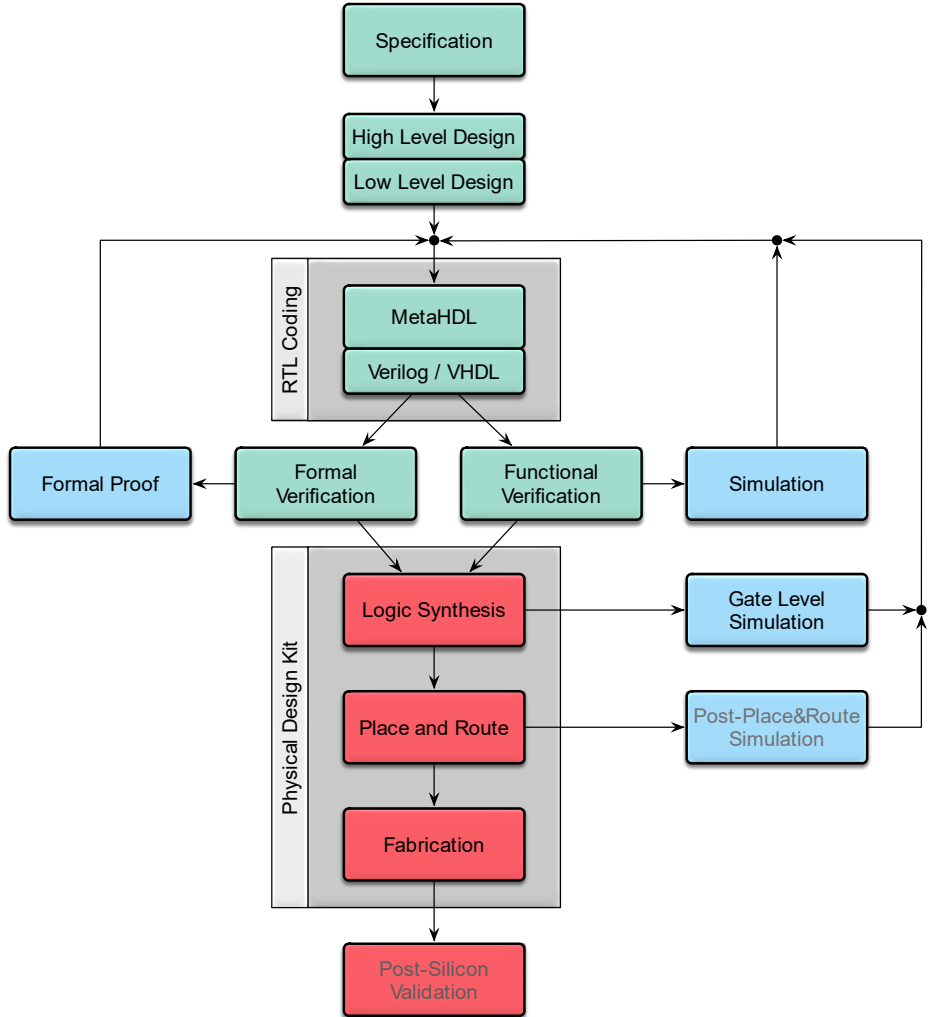Open-source generates innovation by sharing knowledge. Hence HEP needs an

- open RISC-V core -- VexRiscv
- open (meta-) HDL -- SpinalHDL

For a (real) HSM we additionally need

- a free toolchain -- OpenROAD/OpenLane
- a compatible PDK for fabrication

Goals:
- everybody can verify & correct our design
- no backdoors
- more competences in ASIC manufacturing

Open EDA Chain

- Based on Google/Skywater130 „an experimental preview"

  - We implement by integrating proprietary input from IHP PDK
  - Ongoing work on OpenROAD/OpenLane chain (open-source)

- Modified SpinalHDL

  - Include (semi)-automatic countermeasures

  - Enable formal verification

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OpenROAD/OpenLane

OpenLane

- full open-source flow

- using the PDK by IHP

- open standard formats
  (LEF/DEF/SDC/GDSII)

- TCL scripting

- unsatisfactory steps can
  easily be replaced

The OpenLane Flow
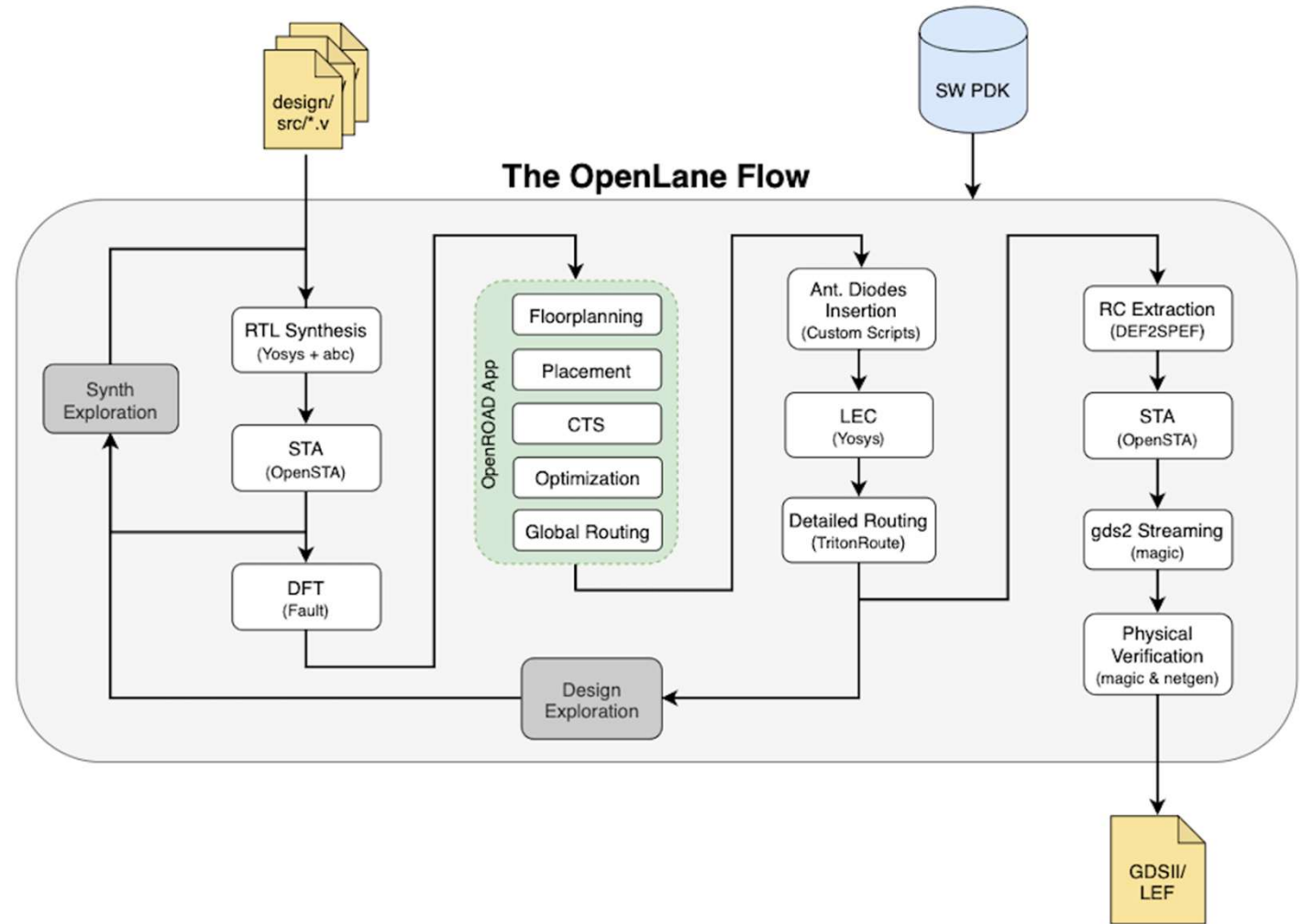
Is OpenLane a Useful Approach?

- **EDA-tools are extremely expensive**

  - This prevents innovation in certain areas

  - Sharing knowledge is difficult

An open-source toolchain surely can't just be as good?

- Correct. If you work with state-of-the art processes (2nm, high-frequency) OpenLane won't do.
  But: In the long run, the community will help!

- However, if you use a bigger, slower process with the goal of robustness, openness and cheapness, OpenLane is already worth the try.

Current Status

- Already added IHP PDK into OpenLane (first GSDII generation)
    - Ongoing effort (DRCs still missing)

- Plan to provide (ASAP) open HSM-code for FPGA (prototype)

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Thank you for your attention!

For more information:

`https://hep-alliance.org/`

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