THE EUROPEAN REFERENCE FAB

Blueprint for a Trusted and Transparent Manufacturing Network

Exposé:

The Transparent Reference Fab (TRF) is a modular 300-mm blueprint (130 → 65 nm, Packaging-First) with open PDKs, auditable processes, and a Comply-to-Connect label. It scales as a network of clonable fabs, monetises via trusted-premium and advanced-packaging services, and remains voluntary and EU-law compliant in its co-operation. Tranche-based financing links disbursements to milestones (construction/tool IQ/OQ, PDK/MPW, audit go-live, 65-nm release); governance options (PPP, SPV, foundation; private with a public-service mandate) remain open. Phase 0 validates site, CAPEX/OPEX corridors, demand anchors (LTAs/Take-or-Pay), and the RefFab Academy. Recommendation: establish an EU task force within 6–12 months to pilot; in parallel, industry MoUs for MPW and a packaging pilot.
All figures are corridors; validation occurs in Phase 0.

Packaging-First. Trusted by Design.

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Content

Transparent Reference Fab for Europe: Open, scalable semiconductor manufacturing as a strategic concept

Executive Summary

Europe faces, in 2025, the existential task of strengthening its technological sovereignty in semiconductor manufacturing. The European Chips Act of 2022 set the goal of increasing Europe's share of global chip fabrication by 2030 from under 10% to 20%—an ambitious undertaking intended to mobilise a total of around 43 bn € in investment[1]. Meanwhile, all 27 EU Member States, under a Semicon Coalition, are calling for an evolution towards a "Chips Act 2.0". Rather than focusing on market share alone, this aims to close critical gaps: secure key technologies, accelerate permitting procedures, and deepen competencies along the entire microelectronics value chain[2]. In parallel, the EU Agency for Cybersecurity (ENISA) warns of increasing cyberattacks on critical infrastructures—a wake-up call that trustworthy, auditable hardware has become a security imperative. Worldwide, other industrial nations are pushing ahead with semiconductor expansion: Japan is investing billions in the Rapidus initiative (target: 2-nm mass production by 2027)[3], and the United States launched the CHIPS and Science Act (52 bn $), followed by major investments such as Texas Instruments' plan exceeding 60 bn $ for new fabs in Texas and Utah[4,5]. China, too, has been flooding the sector with subsidies for years to build domestic fabs. Within Europe, there are isolated initiatives—e.g., Ireland's "Silicon Island" strategy (national semiconductor offensive since 2025)[6], the Swiss "Chip FabLab" project co-led by ETH Zurich[7], or plans around CSIC/CNM in Spain. These individual efforts matter but, lacking critical mass, cannot solve the root problem. Europe must consolidate its strategy and act as one to be prepared against geopolitical risks, supply bottlenecks, and

[1] https://commission.europa.eu/strategy-and-policy/priorities-2019-2024/europe-fit-digital-age/european-chips-act_en

[2] https://digital-strategy.ec.europa.eu/en/news/semicon-coalition-calls-reinforced-chips-act

[3] https://www.rapidus.inc/en/tech/te0006

[4] https://bidenwhitehouse.archives.gov/briefing-room/statements-releases/2022/08/09/fact-sheet-chips-and-science-act-will-lower-costs-create-jobs-strengthen-supply-chains-and-counter-china

[5] https://www.ti.com/about-ti/newsroom/news-releases/2025/texas-instruments-plans-to-invest-more-than--60-billion-to-manufacture-billions-of-foundational-semiconductors-in-the-us.html

[6] https://enterprise.gov.ie/en/publications/silicon-island-a-national-semiconductor-strategy.html

[7] https://ee.ethz.ch/news-and-events/d-itet-news-channel/2025/08/boosting-swiss-semiconductors-plans-for-chip-factory-gain-media-attention.html

technological lag. Against this background, this paper presents the concept of a Transparent Reference Fab as a proactive response.

The Transparent Reference Fab for Europe is a proposed reference semiconductor plant designed to be open, scalable, and production-ready. It serves as an open-source blueprint for the rapid build-out of additional fabs in Europe. Core principles of this approach are:

• **Series-capable manufacturing model instead of a pilot line:** Unlike typical pilot lines (which often have a demonstration character and, at best, capacities for small-series production), the Reference Fab is designed from the outset for industrial volumes and 24/7 operation. It is intended to shoulder real production loads and operate economically, so that any plant copied from this model is production-ready from day one and does not require a costly transition from pilot to series production.

• **Transparent open-source blueprint:** All key processes, equipment parameters, and fab operations are, in principle, openly documented and made accessible for re-use. This transparency allows European industrial actors and states to use the fab as a blueprint to build new plants autonomously with lower development risk. It also creates trust in the chips produced: security-relevant semiconductors can be examined down to the process level, ensuring trusted electronics “Made in Europe”. Any backdoors or manipulations are significantly harder to conceal in a transparent manufacturing process. **Open-PDK & open-source EDA:** Based on open PDKs and reproducible, auditable toolflows (CI/CD), reference IPs and assembly design kits are provided; this measurably lowers entry barriers and audit times. The project thus aims for the **“Trusted EU Fab Network”** label—independent bodies should **certify the trustworthiness** of production on the basis of the open documentation and inspections.

• **Packaging-First & chiplet-readiness:** Performance, energy, reliability, and security targets are now decided in the back end/SiP/SoP. Therefore, advanced packaging is a core component from day 1: RDL/fan-out, interposer/2.5D, and co-packaging of leading-edge compute dies with 65-nm periphery (PMIC, mixed-signal, sensor IF). We anchor chiplet standards (e.g., UCIe/BoW/OpenHBI), design-for-packaging, and qualified test flows (KGD→SLT). In this way, we do not widen the gap to the leading edge but bridge it systemically. Close exchange with EU-funded pilot lines (e.g., APECS) is required here.

• **Focus on 65-nm CMOS as a strategic technology node:** The Reference Fab targets the established 65-nm node, as it is future-proof and sufficiently performant for many critical applications. Sectors such as automotive, industrial, med-tech and aerospace can manufacture their microcontrollers, ASICs and mixed-signal components at 65 nm—robustly, cost-effectively, and in high volumes. Forecasts indicate that even after 2030, a significant share of global chip demand will fall to technologies ≥65 nm (especially analogue/power electronic chips), while <10 nm accounts for only ~12%. As a bridging technology, operations will initially start on the proven 130-nm node, for which equipment and open process data and PDKs are immediately available in Europe. This bridging approach enables a rapid start of production with high yield, while the 65-nm line is ramped

in parallel to maturity. The fab infrastructure is designed modularly so that a later upgrade to 65 nm (or smaller) is possible without fundamental replanning. The focus initially remains on 65 nm as the “sweet spot” between maturity, availability, and sovereignty gains. Importantly, selected platforms will be assured long-term availability (target corridor ≥ 15 years) with obsolescence pathways; certification and qualification pathways (e.g., AEC-Q100/IEC 61508/DO-254) are part of the offering. This explicitly avoids a commodity-volume model and instead pursues a trusted-premium approach with service and quality premiums.

• **Data-driven manufacturing, audit trails & automation:** Dense inline metrology, SPC/ML-assisted control, and end-to-end feedback from front-/back-end data shorten ramp-ups and create verifiable quality and trust metrics; this also includes robotics-based automation processes. Where sensible, selective single-wafer steps are used; furnace/batch processes remain economical.

• **Use of existing resources and expertise:** The Reference Fab should be located in close physical proximity to existing research and pilot lines such as IHP, CEA-Leti, or imec in order to translate existing process know-how directly into industrial implementation. This proximity enables a significantly accelerated ramp-up, as established teams, qualified equipment, and proven process modules can be used directly. At the same time, the Reference Fab remains institutionally independent—it is not an extension of a research institution but an industrial Reference Fab with its own mandate. By purposefully integrating research know-how into an open production model, Europe can become operational more quickly without starting from zero.

• **Governance & public-trust mandate (PPP):** Public ownership or a public-trust mandate—institutionally independent of R&D institutions, with physical proximity/co-location; non-discrimination, open audit interfaces (traceability down to lot/wafer level), clear access rules; industry co-investments in equipment/packaging. This ensures replicability, planability, and verifiable trust mechanisms.

• **Talent, training & trusted personnel (RefFab Academy):** The Reference Fab embeds qualification as a core task. The RefFab Academy provides core curricula, EQF-aligned micro-credentials, and a Skills-Passport directly linked to RBAC/Comply-to-Connect in the MES. Packaging-First (SiP/UCIe, RDL/fan-out, ATE/SLT) starts on day 1; training is delivered via standardised Learning Cells and a “learning-workshop-in-a-box” (on-/off-the-job, bootcamps, VR/AR, digital twin). Dual/VET and higher-education pathways are connected via MoUs to existing programmes; rotations (fab/OSAT/R&I) shorten time-to-competence. Active recruiting (EU programmes, reskilling, international hiring) is flanked by family-ready offers (shift-compatible childcare, language tracks, mentoring; Just-Culture). GDPR-compliant, risk-based background checks and a compliance gate (antitrust/FDI/dual-use/IP/privacy) safeguard publications and artefacts. Open PDKs/EDA and freely available ADKs plus MPWs remain the instructional foundation. Target corridor per Reference Fab in the build-up phase: 30–50 engineers and 70–120 technicians/operators p.a.; long term: ~20 and ~60 p.a., respectively (site-specific validation in Phase 0).

• **Scalable reference solution & network concept:** The overarching goal is a multiplicative effect: the Reference Fab serves as a blueprint that can be copied one-to-one and rolled out across several European regions. Each new fab built to this model immediately increases regional manufacturing capacity and supply-chain resilience. By standardising the architecture, even production lots and personnel can be exchanged between sites. If a fab fails in a crisis situation, others with identical equipment can temporarily step in—improving supply security. Such a network of identical, trustworthy fabs would reduce Europe's dependence on non-European suppliers while also serving as a platform for innovation (e.g., joint further development of new process modules, open IP libraries).

• **Specialisation for niche products:** Multiple fabs with an identical CMOS base can purposefully differentiate themselves through process-modular add-ons (e.g., RF, power, sensor modules, photonics)—without changing the base technology. In this way, we combine economies of scale with technological differentiation in higher-margin niches. The result is a flexible manufacturing ecosystem that promotes both innovation and specialisation in niche markets.

• **Demand anchors:** Public procurement (critical infrastructure/public administration/security) secures base load; industry co-investments lift packaging/test capacities. Delineation: no EUV/leading-edge foundry, no commodity volume model—focus on trusted-premium, SiP/chiplets, and long product life cycles.

• **Financing & economic viability (brief overview):** PPP structure with public base load and industry co-investments; subsidised share of CAPEX (site/EU programmes); staged funding tied to milestones (MPW start, 65-nm ramp, packaging pilot); revenue mix: foundry, packaging/test, services (MPW, certification, obsolescence management).

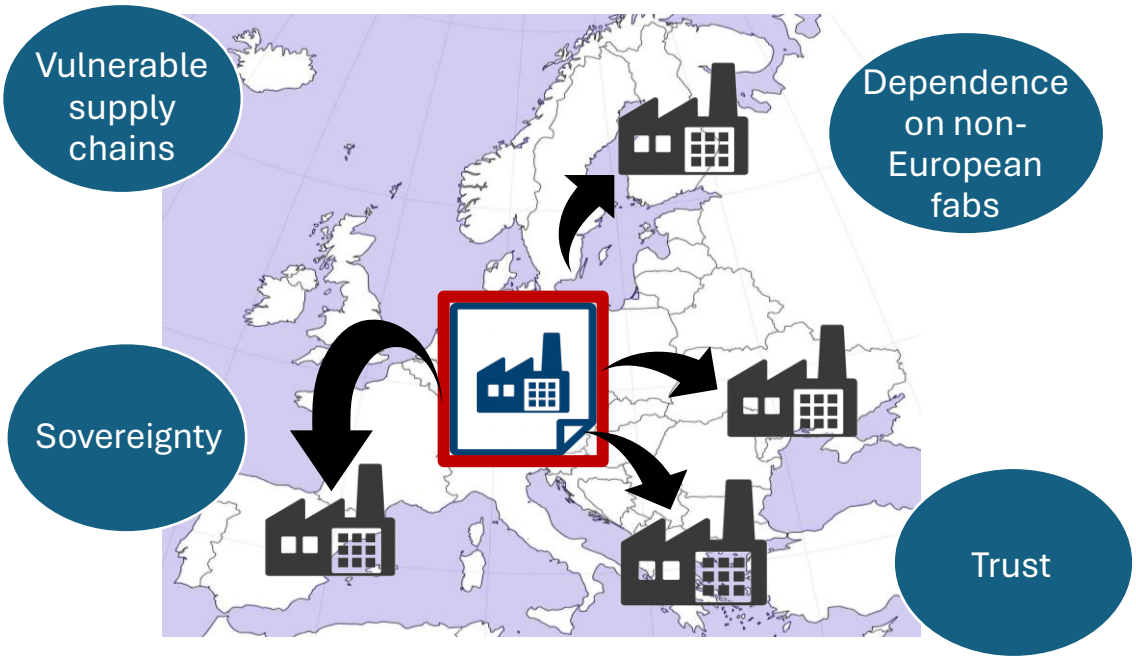
• **Guardrails (without hard promises):** MPW ≥ 4/year (130 nm) & ≥ 2/year (65 nm), SiP-MPW from Year 2; packaging targets: RDL pitch 10 → ≤ 5 µm, microbump ≤ 55 µm; long-term supply ≥ 15 years; trust KPIs: published yield/DPPM & traceability metrics.

Perspective 2040+: The relevance of ≥ 65-nm classes will persist well beyond the 2030s due to analogue/mixed-signal content, power electronics, eNVM MCUs, RF front-ends, rad-hard/space electronics, and security requirements. Long-lifecycle industries (automotive/automation/med-tech/aerospace) and chiplet architectures further stabilise demand: 65 nm takes on peripheral functions, sensing, PMIC, safety MCU, while leading-edge compute is integrated via co-packaging. The network can—where sensible—shrink modularly or expand its SiP/OSAT footprint without changing the business model.

This Executive Summary addresses policymakers at EU and national level as well as potential funders in public administration and industry. It outlines, in compact form, the vision of a Transparent Reference Fab and its benefits. The recommendation is to advance this strategic concept swiftly with political backing and initial funding. In view of the ongoing reform efforts around the Chips Act, the heightened threat environment, and global

investment dynamics, now is the right moment to lay the foundations for open and sovereign semiconductor manufacturing in Europe.

Note (disclaimer): This paper presents a concept and sketches initial proposals for implementation and financing. Delivering a robust realisation will require deeper analysis and a detailed execution plan. Developing these is an integral part of the concept and the subject of Phase 0.



Assumptions, Scope & Non-Goals

- This paper proposes a **replicable Reference Fab blueprint** (capabilities, governance, training) — **not** a site decision or investment commitment.
- Core focus: **packaging-first** (SiP/RDL/Fan-Out), **test/ATE/SLT**, open PDK/EDA integration, **auditability**, and **workforce** pipelines.
- Technology path: **130 → 65 nm** as *evergreen* nodes for AMS/MCU/PMIC/RF/IoT; concrete volumes/product mixes are **partner-specific**.
- Complementary to leading-edge fabs; aims at **resilience, qualification, and SME access**, not volume competition.
- Implementation is **phase-gated** (Phase-0 → Go/No-Go) with measurable milestones.
- Quantitative ranges are **scenario-based**; all figures are indicative pending partner due diligence.

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List of Abbreviations (Executive Summary)

Abbreviation	Meaning
ADK	Assembly Design Kit
AMS	Analogue and Mixed-Signal
ATE	Automated Test Equipment
CAPEX	Capital Expenditure
CD/CI	Continuous Deployment / Continuous Integration
ENISA	European Union Agency for Cybersecurity
EQF	European Qualifications Framework
FDI	Foreign Direct Investment
IP	Intellectual Property
IQ/OQ	Installation Qualification / Operational Qualification
KRITIS	Critical Infrastructure (German: *Kritische Infrastrukturen*)
LTAs	Long-Term Agreements
MES	Manufacturing Execution System
ML	Machine Learning
MoU	Memorandum of Understanding
MPW	Multi-Project Wafer
OPEX	Operational Expenditure
OSAT	Outsourced Semiconductor Assembly and Test
PDK	Process Design Kit
PMIC	Power Management Integrated Circuit
PPP	Public–Private Partnership
RBAC	Role-Based Access Control
RDL	Redistribution Layer
SiP	System-in-Package
SLT	System-Level Test
SoC	System-on-Chip
SoP	System-on-Package
SPC	Statistical Process Control
SPV	Special Purpose Vehicle
TRF	Transparent Reference Fab
UCIe	Universal Chiplet Interconnect Express
VET	Vocational Education and Training
WSPM	Wafer Starts per Month

Starting point: sovereignty under new conditions

Over recent decades, Europe has lost substantial ground in semiconductor manufacturing. At present, less than 10% of global chip production is accounted for by European fabs. High-value microelectronics largely originate from Asia or the United States—particularly at the leading edge, Europe is almost entirely dependent on imports. Over 80% of advanced chips used in areas such as AI, telecommunications, med-tech, or defence must be imported from the United States or East Asia[8]. This concentration is not only an economic issue but also a strategic risk: supply disruptions (for example, due to geopolitical tensions around Taiwan) could paralyse essential industries. The COVID-19 pandemic and subsequent chip crises painfully exposed the vulnerabilities of global supply chains.

Against this backdrop, the EU adopted the European Chips Act in 2022 to counteract these trends. The official goal was to double Europe's global market share to 20% by 2030—with public incentives and regulatory facilitations intended to trigger investments of over 40 bn €. In practice, an investment wave has indeed been set in motion, yet doubts are growing about achieving the 20% target. The European Court of Auditors (ECA), for instance, considers the target excessive and unrealistic—it forecasts that, without a course correction, Europe will account for only around 12% of global value creation in the chip industry by 2030[9]. Accordingly, all EU Member States and industry associations are now pushing for a "Chips Act 2.0": the revision should set clear priorities for where and why Europe must lead in future, rather than merely aiming at an aggregate market share.

At the same time, the threat landscape is intensifying: ENISA and others warn that attacks on digital infrastructure are increasingly targeting hardware vulnerabilities and supply chains. Without trustworthy domestic manufacturing, Europe could become a vulnerable single point of failure in the global technology system. Hardware security "by design"—for example through transparent, auditable production processes—has become the order of the day.

Internationally, there is an intense race for semiconductor capacity. In addition to its 52 bn $ support package, the United States has already seen concrete mega-projects: Texas Instruments is investing over 60 bn $ in seven new fabs in Texas and Utah, while Intel, TSMC, and Samsung are building "megafabs" in Arizona, Texas, and across the US Rust Belt. China has for years subsidised tens of billions for new plants. Japan has formed Rapidus, a consortium (including Toyota, Sony, SoftBank) aiming—with state support (planned 5 tn ¥, approx. 33 bn € required)—to produce 2-nm chips in series from 2027[9].

Europe, too, has recently announced several lighthouse projects: for example, STMicroelectronics and GlobalFoundries are jointly investing in a new 300-mm FD-SOI fab

[8] https://www.eca.europa.eu/ECAPublications/SR-2025-12/SR-2025-12_EN.pdf
[9] https://www.reuters.com/technology/tsmc-begins-producing-4-nanometer-chips-arizona-raimondo-says-2025-01-10/

in Crolles (France)—with ~7.5 bn € in costs planned, of which ~2.9 bn € publicly funded[10]. However, this project was put on hold in mid-2025 due to cyclical headwinds[11]. In Germany, with TSMC as technology leader, the European Semiconductor Manufacturing Company (ESMC) is being built in Dresden. Over 10 bn € is to be invested; in August 2024 the EU approved 5 bn € in funding[12]. This first European TSMC fab (planned for 28/22-nm automotive technology) is to go into production by 2027 at the latest[13] and reach full capacity by 2029[14]. The project is celebrated as a milestone, yet its scope also underlines the challenge: it ties up enormous resources and primarily addresses the 22-nm segment; for truly security-critical nodes >65 nm it brings little direct benefit. Meanwhile, Intel, after protracted wrangling over subsidies, completely cancelled its originally larger project in Magdeburg (~€30 bn for 4/3-nm fabs) in July 2025[15].

In summary, the starting position shows an acute need for new, complementary strategies beyond the previous focus on the very finest nodes. Europe requires additional manufacturing capacity in pertinent technology domains away from the leading edge—and this capacity must be trustworthy, resilient, and rapidly multipliable. This is precisely where the concept of the **Transparent Reference Fab (TRF)** comes in, as elaborated below. It is conceived as a response to sovereignty deficits, security risks, and market gaps in the "legacy" segment, without losing sight of linkages to state-of-the-art developments (chiplets/packaging). Instead of isolated stand-alone solutions, it offers a European, coordinated reference approach.

A concise example illustrates the added value of acting together: applied to the EU, it would be more efficient to develop a scalable reference model that is then replicated at multiple sites, rather than each country building a small semiconductor line in isolation. National solo efforts may yield a short-term boost in local competence but risk duplication of work and fragmentation of resources. An EU-wide reference model—the Transparent Reference Fab—could counteract this by developing best practices centrally and then rolling them out locally. Initiatives already planned (for example in Ireland, Spain, or Switzerland) could be harmonised if they built on the TRF's open documentation and became part of a European network. Rather than operating in separate silos, these pilot projects could thus serve as the first nodes in a European federation and benefit from joint developments. Europe-wide coordination would also increase political clout—instead of many small voices, a concerted approach to funding and industry partnerships would emerge. National initiatives demonstrate Europe's strong willingness to rebuild its own

[10] https://gf.com/gf-press-release/globalfoundries-and-stmicroelectronics-finalize-agreement-for-new-300mm-semiconductor-manufacturing-facility-in-france/
[11] https://bits-chips.com/article/st-gf-fdsoi-fab-paused-among-market-headwinds/
[12] https://ec.europa.eu/commission/presscorner/detail/en/ip_24_4287
[13] https://pr.tsmc.com/english/news/3049
[14] https://ec.europa.eu/commission/presscorner/detail/en/ip_24_4287
[15] https://www.heise.de/en/news/Intel-gives-up-Magdeburg-fab-and-announces-end-of-foundry-10499170.html

manufacturing capacity. To unlock the full potential, however, these efforts should be coordinated and designed for scale. The TRF concept provides a proposal for this: it can serve as a reference framework to interconnect national projects as parts of a larger whole. In this way, a scalable, EU-wide model emerges instead of many isolated pilot factories—more efficient and more resilient in the long term. As a representative of ETH Zurich aptly put it, "it is more cost-efficient to consolidate infrastructure than to operate numerous replicated versions within the country"[16]. This principle can be applied to Europe as a whole to turn fragmentation into alignment.

Conclusion on the starting position: The need for a new, complementary strategy is evident. Europe requires additional semiconductor manufacturing in key technology areas beyond the very finest structures—and it must be trustworthy, resilient, and rapidly multipliable. This is precisely where the concept of the Transparent Reference Fab comes in: as a response to the sovereignty gaps, security risks, and market weaknesses outlined in the realm of established technologies, and as a driver of innovation for new forms of cooperation and openness in microelectronics.

Objectives of the concept

The vision of the **Transparent Reference Fab (TRF)** pursues two overarching objectives:
(1) the rapid multiplication of European semiconductor fabs, and
(2) the assurance of trustworthy production for safety-critical applications.

To achieve these guiding objectives, the concept follows several interlinked sub-objectives:

• **Strengthen technological sovereignty:**
Europe should be enabled to manufacture essential chips autonomously—especially those required in critical infrastructures, the military, or strategic industries. This independence from non-European suppliers increases resilience to geopolitical tensions, export restrictions, or deliberate supply cut-offs.
A key lever is the rapid build-out of additional manufacturing capacity at established technology nodes (≥ 65 nm). Chips in this segment—such as microcontrollers, mixed-signal ASICs, or sensor SoCs—are central to many industrial applications and have recently often been a bottleneck in Europe.

• **Multiplier for new fabs:**
The TRF serves as a reference model that investors and industry can use as a proven blueprint for additional plants. The open blueprint lowers entry barriers for consortia or companies considering their own fab. Every euro of public seed funding into the TRF can mobilise a multiple of private follow-on investment (multiplier effect). Over time, this

[16] https://ee.ethz.ch/news-and-events/d-itet-news-channel/2025/08/boosting-swiss-semiconductors-plans-for-chip-factory-gain-media-attention.html

creates a network of like-for-like fabs with compatible architecture and process bases—sharing common standards and learning from one another.

• **Increase the trustworthiness of electronics:**
A central goal is to build a trustworthy supply chain for electronics "made in the EU". From the production equipment and process know-how to the finished chip, end-to-end auditability should be ensured. The aim is a **"Trusted EU Fab Network"** label, awarded by independent bodies on the basis of transparent documentation and regular audits. Safety-critical applications—from power grids to space—can thus rely on certified, verifiable hardware.

• **Strengthen European networking and resilience:**
The TRF is the starting point for a Europe-wide network of interoperable fabs. Standardised processes and equipment enable mutual backup in crises (failover capability), the exchange of personnel or lots, and joint further development. This raises supply security and reduces systemic dependencies.

• **Establish an open innovation and training ecosystem:**
By openly providing process knowledge (open technology), PDKs, reference designs, and even bills of materials (BOMs), an innovation-friendly environment emerges. Universities, start-ups, and SMEs can plug in directly, develop new designs, or contribute process modules. The fab becomes a practical learning site for students, professionals, and career-changers. In combination with the **RefFab Academy**, a training infrastructure is created that specifically qualifies personnel for packaging, test, data analytics, and fab operations. As in open-source software, collaboratively developed improvements enhance the competitiveness of the entire network.

• **Enable a sustainable business model:**
In the long term, the resulting fabs should operate on a commercially sound basis, ideally without permanent subsidies. The focus is on market segments where quality, trust, and long-term availability command price premia—for example automotive, aerospace, or safety-critical IT. "Trusted chips" from European fabs should establish themselves as a premium product with added value. At the same time, these fabs are part of European infrastructure. This requires a baseline public commitment to safeguard strategic capacity—e.g., via public demand (critical infrastructure), moderate modernisation grants, or regulatory stability. The concept targets a **hybrid model**: market-viable in normal operation, with flanking public backstops in critical phases.
Thus, a hybrid model emerges—**commercially viable in steady state, with public backing as part of Europe's public-service provision**.

In summary, these objectives are tightly interwoven: technological sovereignty builds trust; trust is a precondition for market acceptance; and market success attracts new investors, easing the network's expansion. The TRF therefore addresses **security and scaling in equal measure**—a differentiator compared with conventional fab projects. The TRF is

more than a production site: it is a strategic lever for Europe's sovereignty, innovative capacity, and trust gains in global competition.

Technological roadmap: from pilot to network fab

Building a European **Reference Fab** is a technically and administratively highly complex undertaking. The following roadmap sets out an ambitious yet realistically achievable timeline, grounded in experience from European semiconductor projects. It accounts for regulatory procedures, technological development paths, and parallel acceleration measures. The planning conservatively assumes framework conditions in Germany—deliberately chosen as a robust reference case for permitting and infrastructure matters.

Phase 0 – Feasibility studies and consortium formation (9–15 months)

In this initial phase, the concept, partners, and governance structure are finalised. This includes site analyses (including local construction and environmental requirements), a robust cost estimate, personnel demand and competence analyses, the set-up of a training network, and the definition of the fab architecture including packaging and test infrastructure (e.g., RDL, interposer, SLT/ATE). Proximity to existing research facilities (e.g., IHP, CEA-Leti, imec) is deliberately sought—while maintaining clear institutional independence.
All time and financial figures in the concept are preliminary assumptions and will be validated, prioritised, and specified in this phase.
Target state for Phase 0: Consortium, site decision, financing model, and governance draft are agreed, including a defined scope for integrated packaging from the start of production.

Phase 1 – Construction of the Reference Fab and parallel process development (30–36 months)

Part 1: Planning, permitting, and construction of the fab (24–30 months)
Following completion of the feasibility study, the construction and equipment phase begins. Typical permitting procedures (e.g., under the Federal Immission Control Act—BImSchG—and environmental requirements) are taken into account. To save time, an existing or expandable cleanroom site (brownfield) should be used. The fab is designed from the outset with 300-mm equipment and 65/(55)-nm-capable tools. Space, utilities, and equipment layouts for back-end processes (advanced packaging) are already considered in the base architecture. The concurrent build-up of a packaging zone with chiplet, RDL, fan-out, and interposer capabilities is part of the fab design.
Target state, Part 1: Cleanroom structures, utilities, and main tools are installed and qualified.

Part 2: Parallel process and documentation preparation (30–36 months)
In parallel, existing process recipes for 130 nm are consolidated in partner lines (e.g., IHP,

CEA-Leti, imec) and prepared for 65 nm. The aim is a modular documentation package for the subsequent open-source blueprint. In close coordination with partners, test flows (e.g., KGD → SLT) and packaging-specific process modules are developed, standardised, and qualified. Initial packaging test structures (UCIe, BoW, OpenHBI) are prepared. In addition, this phase launches the concrete design of the **RefFab Academy**: training plans, qualification profiles, and initial learning modules for technicians and engineers are developed.
Target state, Part 2: Complete process documentation for 130 nm; validated pre-versions for 65 nm are available.

Phase 2 – Commissioning of the Reference Fab (9–12 months)

After installation and qualification, production ramp-up starts on 130 nm. Initial test and functional chips are fabricated. Operations simultaneously serve as a proof-of-concept for the transparency principle: MES parameters, yield data, and quality indicators are documented and (to the defined level of transparency) published. In parallel with the ramp, a first packaging test design (e.g., PMIC + test logic) is manufactured and qualified at interposer level. Integration into MES and quality documentation follows the same transparency principles. From this phase onward, the fab is prepared for a certification model under the planned **"Trusted EU Fab Network"** label, which can be validated by third-party assessors along defined transparency pathways.
Target state for Phase 2: Industrially usable 130-nm PDK with test chips and audit documentation is published, plus a verified packaging demonstrator with a documented process route.

Phase 3 – Technological shrink to 65 nm / 55 nm (24–30 months)

Migration to the target 65-nm node begins. Complementary tool upgrades and the transfer of prepared recipes proceed step by step. Multi-project wafers validate the PDK and support yield optimisation. A 55-nm variant can be trialled in parallel. The packaging flows prepared in Phase 2 are now geared towards co-packaging with 65-nm periphery and leading-edge logic. Yield optimisation, thermal simulations, and validation of standard interfaces (e.g., UCIe) are carried out in an integrated manner with the 65-nm ramp-up. Long-term availability (e.g., over ≥ 15 years) and application-oriented certifiability (AEC-Q100, ISO 26262, IEC 61508, etc.) are technically prepared already in this phase.
Target state for Phase 3: Qualified 65-nm process with open PDK, documented yield, and optional co-packaging trial run, plus a qualified co-packaging test chip (SiP or interposer integration) with documented yield and SLT report.

Phase 4 – Networking, scaling, and consolidation (from Year 7–11)

The Reference Fab now serves as a blueprint for additional sites in Europe. First clone fabs are established—ideally based on identical architecture, processes, and PDKs. At the same time, the Reference Fab assumes training and support functions for new teams. The fab's packaging know-how is published as a design-for-packaging guide and integrated into

MPW offerings. New fabs adopt validated packaging flows and adapt them to regional application domains (e.g., sensor integration, med-tech, defence). Access to the fab and MPW services is non-discriminatory and based on transparent access rules (Open Foundry principle).

Structurally, a network of interoperable fabs with shared governance emerges:
• **Community organisation:** coordination of quality, exchange, and further development
• **Open platform:** maintenance and extension of the open process blueprint
• **Audit and certification structure:** adherence to common standards
• **Site diversity:** inclusion of strong clusters (e.g., Dresden, Grenoble, Eindhoven) and structurally weaker regions

Target state for Phase 4: At least three fab sites actively use the reference architecture; community structures and certified processes are established.

Overall timeline

Phase	Period (from project start)	Duration [months]	Target state
Phase 0	H2 2026–2027	9–15	Consortium, site, and financing agreed
Phase 1.1	2027–end of 2029	24–30	Construction & tool installation completed
Phase 1.2	2027–early 2030	30–36	Process & documentation baseline for 130 nm / 65 nm
Phase 2	2030–2031	9–12	130-nm PDK released; production started
Phase 3	2031–2033	24–30	65-nm reference manufacturing validated
Phase 4	from 2031 onwards	long-term	Network & clone fabs in rollout

This plan includes conservative buffers for permitting, tool availability, and process iterations. With political prioritisation, a complete blueprint project cycle can be achieved within **8–11 years**.

Technological guidelines for the fab
Across all phases, the following architecture principles apply:

- **Industrial-grade scalability:** Base module for approx. **5,000 wafer starts per month**; expandable by additional modules to **10,000+**.
- **Modern fab IT setup:** MES, real-time tracking, 24/7 automation, robotics, and advanced analytics for yield optimisation.

- **Open-source PDKs:** Freely available design kits incl. SPICE models, standard cell libraries, and IP blocks for academic and industrial use.
- **Open software infrastructure:** Where possible based on European or open-source software (audits, adaptability, security).
- **Advanced packaging & chiplet-readiness:** From day 1, capacities for RDL/fan-out, interposer, co-packaging (**65 nm + logic**), UCIe support, and qualified **Known-Good-Die (KGD)** flows.
- **Certifiability & obsolescence management:** Technology pathways target long-availability processes with certifiability to industry standards (e.g., automotive, safety).

Roadmap conclusion: The technological roadmap provides a pragmatic, staged path: it enables a rapid start on proven technology, swift migration to the strategic **65-nm** node, and the systematic build-out of a Europe-wide fab network. This approach balances **time-to-market**, **risk minimisation**, and **replicability**—creating the foundation for **technological sovereignty**, **innovation**, and **economies of scale**. Europe can thus produce additional domestic chips in the short term and, in the medium term, establish a manufacturing ecosystem that sets global benchmarks for **security, openness, and resilience**.

Workforce and training strategy

The **Transparent Reference Fab (TRF)** treats people as a strategic lever: **standardised role profiles** with clear levels (Engineer/Technician/Operator, **L1–L3**) and **RBAC** rights in the **MES** anchor **Comply-to-Connect** on the people side; **curricula**, **micro-credentials**, and a **skills passport** make qualification and re-certification measurable and auditable. **Packaging-First** is established from day 1 as its own competence track (SiP/UCIe, RDL/fan-out, ATE/SLT). Development follows transparent paths (technical ladder and leadership) with mandatory leadership fundamentals and mentoring—so scaling does not depend on “hero managers” but on **standards, checks, and audits**. The strategy follows the staged technology roadmap **130 → 65 nm** and enables the fast, reproducible commissioning of identical fabs.

Phase-0 note: The following bandwidths and intake corridors are conservative guide values. Site-specific sizing (automation depth, product mix, shift model), MoUs with education/VET partners, RBAC/re-cert cycles, and the **family-ready** components (see below) are validated bottom-up in **Phase 0** and versioned as a binding part of the blueprint.

Workforce pyramid and FTE corridors (base module ~5 k WSPM)

The organisation rests on eight job families: **process engineering**, **equipment/maintenance**, **production/operator**, **metrology/QA**, **facilities/EHS**,

IT/MES/OT-security, **packaging/test (ATE & SLT)**, and **academy/training**. Demand is phase-dependent. In the ramp, engineering and maintenance roles dominate (tool IQ/OQ/PQ, ramp methodology); in 24/7 steady state, the operator share grows; during 65-nm qualification, load again rises in process and metrology. **Brownfield** lowers time-to-competence and initial FTE peaks (experienced crews, existing SOPs), while **greenfield** temporarily requires higher engineering and training capacity. Shift model and automation level (AMHS/robotics) are designed so that **TtC** is short, **OEE** stable, and **traceability/audit** always ensured.

T1 – Workforce pyramid & FTE ranges (per phase; guide values)

Job family	Ramp-up	SOP 130 nm	SOP 65 nm
Process engineering	15–25	10–15	25–35
Equipment/maintenance	25–40	15–25	25–35
Production/operator	25–40	100–140	120–160
Metrology/QA	10–15	20–30	25–35
Facilities/EHS	10–15	15–20	15–20
IT/MES/OT-security	8–12	10–15	12–20
Packaging/test (ATE/SLT)	10–15	20–30	30–50
Academy/training	6–10	6–10	6–10
Cross-functional & management*	25–40	60–90	80–120

* Procurement/SCM, quality systems, HR/finance, HSE compliance, communications, site services (partly as shared services).

In full operation, headcount for the base module (incl. cross-functional) typically sits around **~350–500 FTE**. For the pipeline, plan **30–50 engineers** and **70–120 technicians/operators p.a.** during the build-up phase (2–3 years); in the steady phase, around **20** and **60 p.a.** respectively.

RefFab Academy (training ecosystem)

The **RefFab Academy** acts as an umbrella with central curricula, trainer certification and a digital learning platform (**LXP**), plus regionally attachable hubs. Unified standards, **EQF-aligned micro-credentials** and a **skills passport** become part of **Comply-to-Connect** (personnel certification in parallel with process audit). Site-independent, replicable **Learning Cells** and a **"learning-workshop-in-a-box"** (outside sensitive cleanroom zones) ensure identical training environments. Partnerships with EU skills initiatives,

VET/chambers, universities, and OSAT/ATE OEMs ensure reach and interoperability; **ECTS/VET mapping** is maintained centrally.

Onboarding combines **6–12-week bootcamps** (cleanroom/EHS, tool basics, yield/metrology), **VR/AR-supported tool training** and **digital-twin simulators** with mentored on-the-job practice. Rotations between the Reference Fab, OSAT partners, and R&I shorten **time-to-competence (TtC)** and broaden practical experience. A **train-the-trainer** path professionalises scaling; **returnships** enable lateral and re-entry. All evidence feeds the **skills passport** and is **RBAC-linked** (re-cert typically **24–36 months**).

T2 – Curriculum matrix & training times (extract)

Module (example)	Target profiles	Format/duration	Completion/re-cert
Cleanroom 101 / EHS/REACH/Seveso	all	Bootcamp **1–2 weeks**	Badge L1 / **24 m**
Litho/Etch/Dep basics	Operator, Maint., Process	Bootcamp **2–3 weeks**	Badge L1 / **36 m**
Yield/FA/Metrology	Process, QA	Course **1–2 weeks**	Micro-cred / **36 m**
MES/Traceability/ISO 27001	IT/MES, line leadership	Course **1 week**	Micro-cred / **24 m**
AMHS maintenance L1 (with AR/VR)	Maintenance	Practice **1 week**	Badge L1 / **24 m**
UCIe & chiplet test (ATE/SLT)	Test/packaging	Course **3–5 days**	Badge / **24 m**
Operator cross-training (litho/etch)	Operator	Rotation **4 weeks**	Micro-cred / **24 m**
Train-the-trainer	Senior specialists	Course **1 week**	Certificate / **36 m**

The **skills passport** captures the sequence **recruiting → bootcamp → mentored on-the-job → L1 → specialisation (packaging/test/IT/MES etc.) → L2/L3** with re-certifications. It also serves as evidence for the **Trusted-label audit**.

Packaging-First tracks and test

In parallel with front-end, from day 1 build **RDL/fan-out**, **interposer/2.5D**, **flip-chip/microbump**, **UCIe/die-to-die**, **SI/PI/thermal**, **KGD flows**, and **ATE/SLT**. The **minimum scope in years 1–2** includes an **RDL/flip-chip cell**, a **basic interposer flow**, an **ATE cell** (with DFT/DFM coupling) and **KGD screening**. This raises **system value per wafer**, ensures **chiplet-readiness**, and reduces dependencies on **OSAT** bottlenecks.

Mobilisation, attraction & retention

Talent acquisition follows an active **sourcing and EVP** strategy: EU programmes (Chips Skills Academy, EIT), dual/integrated study models, **reskilling** from adjacent industries (pharma/optics/battery), **international recruitment** (Blue Card/relocation), and **referral programmes**. **Family-ready sites** increase retention and availability: **shift-compatible childcare** (allocated places with extended hours, back-up care, holiday/camp contingents, voucher/subsidy models, matching service), **language tracks**, and **mentoring** within a **Just-Culture**. Transparent career paths, **tech ladders**, certificate tiers, and a **network-wide badge economy** foster development and mobility; rotations are recognised as development steps. **KPIs** (e.g., time-to-offer, offer-acceptance rate, TtC@90/180 days, pipeline diversity, referral rate) steer effectiveness.

Trusted personnel & compliance (people component of Comply-to-Connect)

The personnel part of the **Trusted label** covers **role-based rights** in the MES (least-privilege), **auditable training/re-cert evidence**, on-/off-boarding processes, and **risk-based, GDPR-compliant background checks** with clear purpose limitation, data minimisation, and short retention periods:

- **L0 – Standard:** identity check, diploma/reference check.
- **L1 – Cleanroom access:** + employment/gap check, passed safety induction.
- **L2 – Critical access** (e.g., MES admin/tool owner): + sanctions/embargo screening, extended references.
- **L3 – Highly critical (security/IP core):** + additional evidence only where legally permissible, **four-eyes** approval.

All checks are vendor-audited (processor agreements) and governed in works agreements/DPIA. The **audit trail** carries **aggregated people KPIs**, without personal details.

The **compliance gate** controls publication/artefacts via defined checks: **antitrust/competition**, **FDI/export/dual-use**, **IP/OSS compatibility**, and **privacy** (anonymisation/pseudonymisation where needed); each release receives a **release ID** and checklist evidence.

KPI set and learning curves

For steering and scaling, use: **time-to-competence**, **quarterly OEE improvement**, **yield-ramp slope (130 → 65 nm)**, **audit score (people part)**, **attrition**, **time-to-hire/offer-acceptance rate**, **referral rate**, **academy throughput**, and **re-cert compliance**. Network-wide **MPWs/qualification runs** and **rotations** generate learning effects that measurably

shorten TtC and ramp time in clone fabs; **training pass rates** and **first-pass yield in learning cells** serve as leading indicators.

Economic leverage and industrial-policy benefits

Beyond its technological and security objectives, the **Transparent Reference Fab (TRF)** has a clear economic-strategy dimension: with a manageable outlay of public funds, additional trustworthy manufacturing capacity on mature nodes is to be created—replicable to generate economies of scale and resilience for Europe—**complementary** to high-end initiatives, not in competition.

Cost efficiency through technology choice and brownfield levers:
A 300-mm operation at 65/130 nm works **without EUV/High-NA**—the single biggest cost driver of modern <5-nm fabs falls away. Reference projects in Europe indicate **CAPEX in the low single-digit billions**; takeovers/refits of existing 300-mm fabs can further reduce time and investment needs. To secure clonability and auditability, **"certified tool families"** are defined (identical model series or quality-equivalent released variants). Refurbished tools are admissible only if they fall within these families and meet the specified process window in a like-for-like audit; otherwise, new equipment is required.

Faster payback via niches and a "trusted-premium" model:
Target segments with higher willingness to pay (e.g., automotive safety/ASIL, aerospace/space-grade, **critical-infrastructure** electronics) carry the trusted model: auditable provenance, long-term availability (10–15+ years), documented quality KPIs, and prioritised delivery in crises justify price premia and stabilise cash flows. Public and semi-public demand anchors (authorities, rail/energy, defence, space) secure base load via multi-year offtake contracts (incl. take-or-pay), readiness/retainer payments, and—where sensible— **critical-infrastructure** sourcing quotas ("EU-Trusted").

Co-operation—yes, voluntary and EU-law compliant:
As an industrial-policy mechanism, the network targets **voluntary, compliant** economies of scale—underpinned by standards, audits, and fundable **pre-competitive** modules. Scale advantages arise voluntarily and in line with competition law: permitted are pre-competitive co-operations with **information hygiene** (e.g., open/standardised open PDKs, modular process/qualification data in aggregated/lagged form, joint MPW runs, framework procurements with firewalls, shared training curricula). **Not** shared: prices/margins, customer-specific capacities/volumes, future output or bidding strategies. **Chips Act/ECIC and IPCEI** mechanisms encourage such collaboration but do not dictate commercial policy. Governance rules ensure trustee/clean-room setups, data classification, opt-in modules, and auditability.

Specialisation of clone fabs: identical base, different niches:
With a common 65-nm CMOS base, archetypes enable differentiation while preserving scale:

- **Automotive safety/ASIL** (AEC-Q100, ISO 26262; long-term availability) for safety-critical MCUs/ASICs,
- **RF/mixed-signal & sensing** (RF-SOI/eNVM) for IoT transceivers, radar front-ends, sensor ASICs,
- **Power & BCD (smart power)** for PMICs, gate drivers, and HV options (130 → 65 nm BCD),
- **Advanced-packaging hub** (RDL/fan-out, interposer/2.5D, co-packaging of 65-nm periphery with leading-edge logic, UCIe interfaces),
- **Aerospace/space-grade** (ECSS/DO-254; radiation-tolerant/hard).

Advanced packaging & chiplet-readiness raise the **system value per wafer**, bridge procured leading-edge logic, and address Europe's gap in the **OSAT/interposer** segment—leveraging both margin and resilience. Politically, specialisation unlocks lead markets, boosts margin stability, and distributes value creation purposefully across regions and sectors.

Ownership/operating models and cross-border scaling:
PPP is one option alongside public **SPV**, foundation/association, cooperative, or private ownership with a public-service mandate. Clone fabs can be operated by different EU states or public enterprises; prerequisites are uniform audit/security requirements, **open-access principles**, and compliance with state-aid/procurement rules. **Non-EU stakes** are considered only restrictively (FDI screening, minority limits, golden-share/trust conditions); core control remains in EU hands.

Regional economic impulses and multiplier:
A **5k WSPM** unit creates several hundred **highly qualified** direct jobs; indirect/induced effects drive a substantial multiplier (suppliers, services, test/OSAT, training). The **distributed blueprint strategy**—combining strong clusters and structurally weaker regions—broadens participation and increases political feasibility. **Obsolescence services** (form-fit-function re-design, mask maintenance, long-term wafer saves) generate recurring revenue and bind customers over the product life cycle.

Site costs realistic—and actively mitigated:
Higher energy/water costs in Europe are addressed via **PPAs** and load management, water recycling/UPW recovery, modular automation (OPEX lever), predictive maintenance (MTBF↑, downtime↓), and a skills academy/dual programmes for talent security. This reduces time-to-yield and overall operating costs. Industrial policy flanks these measures with qualified state-aid frameworks, training programmes, and standardised energy instruments (e.g., PPAs).

Complementarity with high-end initiatives:
The TRF complements 2-nm pilot lines, **ESMC (28/22 nm)**, and other high-end projects: it stabilises value creation, qualifies personnel/suppliers on mature nodes, provides

complementary **advanced-packaging** services, and reduces dependencies in safety-critical supply chains.

Measurability & governance as industrial-policy levers:
Impact and trust are made transparent via **trust KPIs** (e.g., DPPM targets, audit score, level of transparency, lead-time reliability). The **"Trusted EU Fab Network"** label is tied to regular audits, data/IT-security requirements, **tool-family compliance**, and **defined transparency corridors**. **Comply-to-Connect** means: baseline standards (standards/PDKs, audit access, security) are mandatory; beyond that, operators may **opt into** co-operation modules (e.g., procurement, joint qualifications)—**without** exchanging commercially sensitive information.

Conclusion:
The TRF leverages mature nodes and a **no-EUV** approach to keep CAPEX low, monetises added value through **trusted-premium** positioning and **advanced packaging**, and scales via a **voluntary, law-compliant** network—**complementary** to Europe's high-end path. An initial public seed investment can trigger a European **"silicon multiplier"**: new fabs, new business models (e.g., SME-focused foundry services), high-quality jobs, and additional strategic value creation. The crux is to couple technical scalability with smart demand anchors and a viable business/governance model—not as a technical parlour trick, but as the foundation of an industrial movement. The result is a **replicable, long-term competitive manufacturing ecosystem without permanent subsidies** that measurably strengthens Europe's sovereignty, security, and resilience—and gradually reduces dependencies.

Financing and preliminary timeline

Realising the **Transparent Reference Fab (TRF)** requires substantial financial resources—yet, as shown, orders of magnitude below leading-edge fab projects. For a **300-mm base module (~5,000 wafer starts/month)** on **130 → 65 nm without EUV**, a robust corridor can be derived from European comparison projects and market benchmarks. **Important:** the figures given here are indicative; a precise bottom-up calculation will be carried out as part of the feasibility study (Phase 0).

Investment costs (CAPEX)

Investment for a 300-mm facility at 130/65 nm depends strongly on the approach (greenfield vs brownfield), the day-1 packaging scope, and the tool policy (defined **tool families**, quality-equivalent vs refurbished). Current experience suggests the following orders of magnitude:

- **New build (greenfield):** A completely new plant with up-to-date 300-mm infrastructure (buildings, cleanrooms, utilities), a digital backbone (MES/traceability/SecOps), and new DUV-capable process tools typically lies in the

1–2 bn € corridor for a base module (~5k WSPM). Reference anchors: **Bosch Dresden (~1 bn €, start-up 2021)** and **Infineon Villach (~1.6 bn €, 2021)**. [Bosch, 2021; Infineon, 2021]. For higher initial capacities (>10k WSPM) costs rise accordingly. At <7-nm level (EUV), comparable projects are **orders of magnitude higher (>10 bn €)**.

- **Conversion/expansion (brownfield):** Where existing 300-mm infrastructure (buildings, cleanrooms, utilities) can be used or expanded, time and capital needs fall significantly. Depending on asset quality and target node, a solution **well below 1 bn €** is possible. A prominent anchor is **onsemi's acquisition of GF East Fishkill (300 mm, 65/45 nm) for ~430 M $** (plus refit/invest), demonstrating that legacy infrastructure can cut capital needs by a factor of **2–3**.

- **Use of refurbished equipment:** As **~70–80%** of fab investment is process equipment, selective use of refurbished 300-mm tools can bring substantial savings (**typically 30–70%** vs new, depending on generation/availability). For clonability and auditability, however, only **defined tool families** (identical or quality-certified model series) are admissible, with verification of the specified process window in an equivalent audit; otherwise, new equipment.

- **Packaging-First (as a CAPEX block):** An integrated back-end module (RDL/fan-out, interposer/2.5D, flip-chip/microbump, ATE/SLT) is co-planned from day 1 and scaled in phases. Depending on scope, **packaging-readiness adds ~+10–20%** to front-end CAPEX. Benefits: shorter time-to-market for SiP/chiplet solutions, higher value per wafer, resilience against OSAT bottlenecks. European anchors (e.g., advanced-packaging investments in IT) underline the strategic relevance.

Note on scaling: The target capacity of **~60,000 wafers/year (base module)** is deliberately small—modern "gigafabs" achieve multiples thereof. Studies cite an efficient minimum scale for 300-mm logic around **~40k WSPM**; the Reference Fab is therefore **modular by design** (cleanroom, utilities, logistics) and can grow linearly towards **10k+ WSPM** via additional tool clusters/shift models.
"As large as necessary, as modular as possible"—scalability is engineered in without over-investing upfront.

Operating costs (OPEX)

Annual operating costs for a 300-mm facility of this size, at full load, fall in the **high eight-digit to low nine-digit € range**. Key OPEX factors are:

- **Personnel:** For ~5k WSPM—depending on automation and shift model—**several hundred** specialists are required (process/equipment engineers, technicians, operators, quality, logistics, IT). Reference anchor: **Bosch Dresden** reports **~700 employees** at full build-out (with a different product/capacity structure). For the Reference Fab, an initial corridor of **~400–600 FTE** can be assumed.

- **Energy & utilities:** Continuous load in the **double-digit MW** range for HVAC, cooling, vacuum/exhaust treatment, UPW generation, etc. At EU industrial power prices (with PPAs/load management) this results in **tens of millions € p.a.**; added to this are water/wastewater, gases/chemicals (with recovery/abatement). **UPW recycling (30–50%)** and heat-recovery lower medium-term costs.
- **Materials & maintenance:** Bare wafers, resists/developers, process gases (Ar, H_2, N_2, F-gases), etch chemicals, spare parts/service contracts. **Preventive maintenance** and in-house spare pools stabilise MTBF and reduce downtime; as a rule of thumb, **5–10% of tool depreciation p.a.** is a maintenance corridor.
- **Other fixed costs:** Facility management (cleanroom classes), IT/MES/cybersecurity, insurance, waste disposal, licences (where needed).

OPEX orientation (corridors, at ~60k wafers/year):

Cost category	Order of magnitude p.a.	Notes
Personnel	**50–80 M €**	~400–600 FTE incl. shift operation [Bosch, 2021]
Energy & utilities	**15–30 M €**	Power/UPW/gases/chemicals (EU price band, efficiency levers)
Materials & maintenance	**30–50 M €**	Wafers, chemicals, spare parts, service contracts
Other fixed costs	**10 M €+**	Facilities, IT/MES, insurance, waste
Total OPEX	**~100–150 M €**	At full utilisation; higher in ramp years (yield effects)

Context: Wafer prices and manufacturing costs are **significantly lower on mature nodes** than at the leading edge; this improves economics at medium volumes but requires high utilisation and **stable demand anchors**.

Validation via comparison projects

Multiple projects in Europe and internationally confirm the above metrics and provide experiential data:

- **Bosch Dresden (DE)** – 300 mm, 65 nm and above: opened 2021 as a “wafer fab of the future”. **~1 bn €** investment, build time ~3 years (2018–2021), **~700 employees** at full build-out. High automation accelerated the ramp (start ~6 months earlier than planned). **Relevance:** cost framework and timeline for a European 300-mm facility in the mature segment.
- **STMicroelectronics/GlobalFoundries Crolles (FR)** – 300 mm, FD-SOI ~18 nm: announced 2022; target capacity up to **620k wafers/year (~51.6k/month)** at full

build-out. **~7.5 bn €** investment (incl. infrastructure/ramp), **~2.9 bn €** public funding; project **temporarily slowed/paused in 2025** (demand uncertainty). **Relevance:** scale effects & state-aid logic for large mature-node projects; market risk at very high volumes.

- **ESMC – TSMC/Bosch/Infineon/NXP (DE)** – 300 mm, 28–12 nm: started 2024; planned output **~40k WSPM**, investment **>10 bn €**, aid **~5 bn €**. SOP targeted end-2027, full capacity around 2029. **Relevance:** leading-edge scale (significantly more expensive) but illustrates EU aid/timeline logic.
- **Infineon "Smart Power Fab" Dresden (DE)** – 300 mm power: ground-breaking 2023, **~5 bn €** investment, **~1 bn €** funding; start-up from 2026, full build-out 2030+. **Relevance:** more-than-Moore scale and phased expansion.

Financing and institutional anchoring

Realising the **European Reference Fab** requires significant funds yet remains strategically favourable relative to modern leading-edge plants. The following statements are indicative; Phase 0 will validate and specify them.

- **Investment frame & strategy:** The fab is conceived as **European public-interest infrastructure**—with **open PDK**, audit transparency, and **Packaging-First** as **first-of-a-kind** features (eligible for state aid). **Tranche-based financing** ties disbursements to milestones (construction progress, tool IQ/OQ, PDK/MPW start, audit go-live, 65-nm release).
- **Preferred model: PPP (public–private).**
  – **Public sector** (EU, national, possibly regional) covers planning, construction/facility, training, and initial process/PDK development.
  – **Private partners** (industry, suppliers, user sectors) co-invest in equipment, working capital, and co-developments.
  A possible target model is a **European Reference Fab Foundation**, curating operations, standardisation (tool-family policy/PDK), Comply-to-Connect, and the openness of the blueprint (**public-trust mandate**).

Funding sources:

1. **EU programmes:** Chips Act/FOAK, Horizon Europe, EIC, IPCEI Microelectronics/Communication.
2. **National funds:** host-country support (construction, energy infrastructure, training).
3. **Industry consortia:** equity shares/special-purpose vehicles (e.g., automotive, defence, telecom, IoT) in return for quotas/board seats—**without** constraining open access.

4. **European partner states:** co-investments by associated countries (CH/NO/UK) in return for know-how access.
5. **Innovative instruments:** project bonds, green-tech infrastructure funds, public-trust endowments (ESA-analogous) to secure operations.

Long-term financing and scaling: After successful establishment of the first Reference Fab, public support recedes stepwise. **Follower fabs** become increasingly privately/regionally financed; the central entity provides governance, auditing, training, and PDK/MPW maintenance. The result is a scalable, **European-controlled network** that can raise Europe's current **~9%** share of global chip production over time.

Transparency and replication
The complete financial structure (investment, operations, learning curves), **tool-family policy**, and audit/PDK processes become part of the **open blueprint**. Followers (universities, SMEs, clusters) can adapt cost models and set up clone fabs—or parts thereof—subject to **Comply-to-Connect** (audit score, IT/data security, defined transparency corridor). The network learns iteratively (MPW experience, PDK updates, packaging flows), thereby increasing efficiency and resilience.

Demand anchors and revenue logic
To secure base load, multi-year **LTAs** (incl. take-or-pay) with critical-infrastructure actors, automotive-safety/ASIL, aerospace/space-grade as well as **resilience retainers** are concluded. **Trusted-premium** (auditable provenance, long-term availability, documented quality KPIs) and **packaging complementarity** (interposer/2.5D, chiplets/UCIe) stabilise utilisation and margins—especially in the **130-nm ramp phase**.

Legal/governance guardrails
Co-operation within the network is **voluntary and competition-law compliant** (pre-competitive: open PDK/MPW/qualification runs, standardisation, where appropriate procurement pools with firewalls). **Prices/capacities/customer data are not shared. Chips Act (FOAK)** and **IPCEI** set the aid framework; **FDI screening** governs third-country participation (minority limits, golden-share, security governance). Participation in the network follows **Comply-to-Connect** (audit score, tool-family compliance, IT/data security, defined transparency corridor).

Risks and buffers
Top risks: permitting/ESIA/BImSchG, tool lead times, energy-price volatility, skills availability, demand cycles. **Mitigation:** early authority roadmap and brownfield option; MoUs/multi-sourcing for key tools; PPAs/load management; RefFab Academy/dual programmes; LTAs/retainers and **sequenced ramp** instead of big-bang. Schedule buffer of **±6–9 months** in Phases 1–3 and a **budget buffer of ±10–15%** are planned.

Summary
Given the strategic importance and the potential for replication, the investment appears **significant but justifiable**: **greenfield typically 1–2 bn €** for a **5k WSPM** base module (**65-**

nm-capable); **brownfield can be significantly lower**. **Packaging-First** is factored in as a strategic block (additional CAPEX share; higher system value per wafer). The time windows (**SOP 130 nm 2030/31; 65-nm qualification 2031–33**) are realistic and buffered. **Tranche-based financing** links public aid (Chips Act/IPCEI/FOAK) and private capital to milestones (PDK/MPW, audit go-live, 65-nm release). **Transparency** (open PDK, transparency corridor) and **Comply-to-Connect** secure clonability and network effects. The result is a **replicable, long-term viable model**—with comparatively **low capital outlay** and **high impact** on Europe's sovereignty, security, and resilience.

Governance and openness management

The **Transparent Reference Fab (TRF)** combines public-interest objectives, private participation, and open-source principles. To ensure that openness, security, and replicability go hand in hand over the long term, governance must (1) define clear roles and checks-and-balances, (2) consistently comply with EU legal and state-aid frameworks, and (3) make the network capable of learning and auditing.

Ownership, operation, mandate

Separation of ownership and operation: Core infrastructure (buildings, cleanrooms, utilities, OT/IT backbone) is preferably held by a public or non-profit entity (e.g., public SPV/foundation). Day-to-day operations can be carried out by a PPP or a publicly controlled company. In this way, strategic decisions (levels of transparency, audit obligations, tool-family compliance) remain subject to a **public-trust mandate**, while industrial excellence is ensured in daily operations.
Multi-state and cross-border operators: Clone fabs may be operated by different Member States or public enterprises, provided state-aid, export, and security requirements are applied in a harmonised manner (uniform audit path, labelling framework, FDI requirements). Third-country stakes are permissible only under clear governance conditions (e.g., minority limits, golden-share, security side-conditions); core control remains in EU hands.

Blueprint governance (open-source model)

Foundation/association as "custodian of the blueprint": An independent blueprint foundation/association manages documentation, open PDKs, reference process recipes, tool-family policies, and design kits. Membership is open to reference and clone fabs, research, suppliers, and user sectors. The foundation runs versioning and review processes (Technical Steering Committee), issues licences (e.g., open base modules plus an IP pool for optional add-ons), and operates an open issue/change process—analogous to established open-source foundations (e.g., Linux/RISC-V).
Comply-to-Connect: Access to the network (label, MPW slots, exchange formats) requires minimum conformity: (i) audit score ≥ threshold, (ii) tool-family compliance or quality-equivalent models, (iii) IT/OT security baseline, (iv) a defined **transparency corridor**

(publishable artefacts, data latencies). Violations trigger graduated sanctions (from remediation periods to label withdrawal).

Certification, label, and quality

"Trusted EU Fab Network" label: An independent certificate attests process and supply-chain transparency, traceability, security controls, and documented quality KPIs (e.g., DPPM, change-control discipline). Audits are conducted by a neutral, accredited body (EU agency/notified organisation), with regular re-audits and event-driven spot checks.
Measurable trust KPIs: In addition to binary conformity (pass/fail), quantitative indicators are published (e.g., audit-score bands, mean-time-to-patch, share of documented process windows) to enable comparability across the network—without disclosing business-critical detail.

Transparency vs security & export control

Tiered openness ("need-to-know + time lag"): Process and quality data are provided as openly as possible and as protected as necessary: freely accessible base elements (design rules, PDK models, generic process recipes), **label-bound** artefacts (e.g., detailed metrology windows), and confidential elements (e.g., security-relevant recipe parameters) with controlled access and delay/anonymisation.
Export/sanctions compliance: Publication and access to collaboration are checked against the applicable EU dual-use and sanctions frameworks; export/sanctions screening is an integral part of the release process.

Co-operation—yes; voluntary and competition-law compliant

Pre-competitive collaboration: Allowed formats include open-PDK maintenance, joint MPW runs, standardised qualification flows, training curricula and—under strict firewalls—framework procurements (standard chemicals, gases) and jointly financed non-IP-sensitive tools (metrology/facility). Excluded are exchanges on prices/margins, customer-specific capacities/volumes, and future output or bidding strategies.
Governance tools: Antitrust compliance is ensured via data classification, **information hygiene** ("traffic-light" schema), clean-room processes, and independent trustees; all committees receive mandatory antitrust training, minute-keeping, and legal pre-checks.

EU integration and programme alignment

Interfacing with Chips-Act structures: Strategic embedding via the **European Semiconductor Board** (policy coordination) and the **Chips Joint Undertaking** (funding for pilot lines, capacity build-up). The TRF can dock in as an open demonstrator/**first-of-a-kind** without ceding operational control to programme bodies.
State-aid eligibility and programme fit: TRF activities (open PDK, audit path, packaging pilot, training) are mapped to aid-eligible capacity and innovation blocks. Governance

ensures **open spillovers** (blueprint, training, standardisation)—a central condition for IPCEI support.

Dispute resolution and escalation

Multi-stage settlement: (i) Technical disputes: Technical Steering + independent review panels; (ii) governance/label disputes: foundation conciliation board; (iii) site/funding disputes: coordination format with Member States/EU bodies. Contractually embedded: **mediation → arbitration** (institutional, e.g., DIS/ICC), including **interim remedies** (e.g., temporary label suspension).

Continuity, measurability, learning loops

Evidence-based management: Risks (fragmentation, duplication, funding timing) are addressed proactively: regular KPI reporting to the sponsor/EU bodies, an open progress report ("**State of the Blueprint**"), and a public dashboard on label/audit status.
Update cycle: Quarterly blueprint releases (**SemVer**), semi-annual security advisories, annual label re-audits; member **roadmap votes** safeguard legitimacy and planning reliability.
Transparency does not end at the fab: It must be visible through an active, rules-based communication strategy—consistent with governance, legal, and security requirements.

Communications and stakeholder strategy (cross-cutting)

Target image: trust through transparency: Progress, quality, and security of the TRF are communicated proactively, intelligibly, and in a timely manner—without violating protection interests (security/export control).
Audiences: policymakers & authorities (EU/Member States), industry & suppliers, research/education, community/OSS, public/media, critical infrastructures.
Formats & channels:
• **Open-blueprint portal:** versioned documentation (PDKs, process guides, tool-family policy), changelogs, FAQs.
• **Quarterly "State of the Blueprint" report:** roadmap status, audit/trust KPIs, MPW dates, packaging updates.
• **Label register ("Trusted EU Fab"):** publicly viewable audit status (traffic-light/score band).
• **MPW/education communication:** semester slots, academia kits, design challenges.
• **Lighthouse moments:** first silicon, 65-nm release, packaging demonstrator; accompanying tech briefings for policymakers.

Crisis & security communications: Playbook with roles (**SPOC/CSIRT/press officer**), templates (advisories), graded disclosure levels (disclose after fix/workaround), and a binding timeline (e.g., **T+24/72-hour** updates).
Governance embedding: Content sign-off by Technical Steering + compliance check (antitrust/FDI/dual-use). Publications carry a release stamp (**Open / Label-bound /**

Confidential with time lag).
Measuring success: Metrics include portal usage, MPW utilisation, share of external contributions (**pull requests**), audit-KPI trends, reach in policy/industry, and the talent pipeline (Academy intakes).

Phase linkage:
• **Phase 0/1:** brand-building, portal MVP, the "why 65 nm + Packaging-First" narrative, recruiting.
• **Phase 2:** first silicon, 130-nm PDK release, label pilot.
• **Phase 3:** 65-nm release, co-packaging showcase, network onboarding.
• **Phase 4:** network stories, benchmarking, policy briefings on resilience/impact.

Core message: Governance, label, and communication form a single whole: **rules safeguard openness and competition**, **audits make trust measurable**, and **targeted communication** carries outcomes to policymakers, industry, and the public—without breaching security or export requirements.

RefFab as public infrastructure: mandate and state commitment

The **Reference Fab (TRF)** is not merely an industrial project but a system-relevant production infrastructure—comparable to energy and communications networks. It safeguards supply, sovereignty, and resilience in safety-critical value chains. This implies a **public mandate**: the fab is designed for long-term availability, auditability, and crisis readiness—while operating on a market basis under normal conditions.

- **State commitment: public-trust mandate & governance:** separation of ownership and operation, **Comply-to-Connect**, independent **"Trusted EU Fab Network"** label; the state provides the guardrails, not day-to-day management.
- **Base load & standby capability:** multi-year offtake/retainer models (e.g., **LTAs/take-or-pay**, resilience retainers) for critical-infrastructure segments; plannable baseline utilisation without distorting the market.
- **Crisis prioritisation & surge capacity:** clear rules for prioritisation/allocation in emergencies; potentially tested switch-over and ramp-up plans.
- **Support for audits and standardisation:** sustained funding of the open blueprint (open PDK, qualification flows) and the audit/certification pathways as **public goods**.
- **Site and talent dimension:** support for site diversification, training programmes, and a skills academy to reduce personnel risks and dependencies.

- **Economic guardrail: no permanent production subsidy**. The public sector enables (seed support, standards, audits, resilience), while efficiency, customer access, and innovation arise through competition. Thus, the TRF remains infrastructure-like in its safeguards yet **entrepreneurially run**—with clear rules for transparency, security, and replication across the European network.

Risks and mitigations

No innovative major project is free of risk. The key is to recognise risks early and take proactive countermeasures. Building a **Transparent Reference Fab (TRF)** is technologically, regulatorily, and financially demanding. The following risks are considered material; each is paired with targeted **mitigations**.

Permitting, construction, and commissioning risk (timeline)
Risk: Complex procedures (UVPG/BImSchG), environmental and safety requirements, and supply/installation chains can shift SOP. Delays in recent EU projects show the sensitivity of timelines to external factors.
Mitigation: Brownfield preference (existing cleanrooms/utilities); early authority roadmap (scoping workshop, binding schedule); parallelisation (construction/tool orders/PDK work overlap); critical paths with buffer (**± 6–9 months** in Phases 1–3) and contracting with LDs (delay/liquidated-damages clauses).

Equipment lead times and tool classes
Risk: Long lead times, especially for lithography/deposition/metal, with backlogs increasing schedule and cost risk.
Mitigation: Early ordering in Phases 0/1; multi-sourcing within defined **certified tool families** (identical or quality-equivalent audited series); refurbished only if **family-conform** and qualified over defined process windows; safety stocks for critical spares.

Market demand and cyclicality risk
Risk: Cycles (notably in automotive/industrial) and project shifts can depress utilisation and cash flows; the ECA calls for realistic expectation management of EU targets. Competition policy applies.
Mitigation: Demand anchors (multi-year LTAs/take-or-pay in critical-infrastructure/automotive/aerospace); portfolio mix (130-nm ramp products → 65-nm/co-packaging); **MPW** programmes for base load; **specialisation archetypes** per clone fab (ASIL, RF/mixed-signal, BCD, space; cf. ES); **trusted-premium** pricing model.

Energy/utilities and site-cost risk
Risk: Electricity, gas, water, and chemical costs vary strongly by site; volatility can blow through OPEX bands.
Mitigation: PPAs/load management; water/UPW recycling (**30–50%**); waste-heat utilisation; predictive maintenance (MTBF↑, downtime↓); modular automation and power/water redundancies in facility design.

Skills and competence risk
Risk: Shortages of technicians/engineers; competition for talent in EU clusters. European programmes point to substantial needs. (SEMI+1)
Mitigation: RefFab Academy (dual programmes, reskilling, e-learning); co-operation with **ECSA/Chips Skills Academy**; EU visa/mobility corridors; early bonding (scholarships/internships); standard curricula (PDK/packaging training) for network partners.

Cyber, supply-chain, and OT-security risk
Risk: Rising attacks on supply chains, industrial controls, and firmware threaten integrity/availability; ENISA highlights OT/supply-chain as a growing threat landscape. (Strategic Energy Europe)
Mitigation: Security-by-design (zero-trust network, hardened MES/tool PLCs); SBOM/traceability down to lot/tool level; threat-intel sharing across the network (pre-competitive); regular red-team tests; audit trail as a component of the **Trusted** label.

Export-control/FDI/legal risk
Risk: Third-country stakes, component/know-how exports, and shifting sanctions regimes can affect supply and governance structures. (Wolters Kluwer Legal Blogs)
Mitigation: FDI-screening policy (minority limits, golden-share); export-control compliance (dual-use checks, end-use controls); EU-based cloud/IT sovereignty; contractual clauses on location and IP anchoring.

State-aid and governance non-compliance
Risk: Lack of tranching/transparency endangers aid eligibility; the Chips-Act regime requires clear evidence logic (FOAK/resilience). (EUR-Lex)
Mitigation: Tranche-based financing (construction/MPW start/65-nm release/packaging pilot); KPIs (audit score, yield milestones, open-PDK releases); **Comply-to-Connect** as entry condition; audit/revision rights for funders.

Antitrust and information-exchange risk in the network
Risk: Unlawful exchanges (prices, customer-specific capacities, bidding strategies) jeopardise co-operation. The Horizontal Guidelines set tight limits for joint purchasing/standardisation.
Mitigation: Pre-competitive only (open PDK, MPW flows, qualification data in aggregated/lagged form); clean-team/firewall setups; standardisation committees under independent stewardship (blueprint foundation); mandatory training for all partners.

Environmental/sustainability and public-acceptance risk
Risk: Impacts on water/energy balance, chemicals logistics, and land use face high societal sensitivity.
Mitigation: Transparency KPIs (water/energy intensity, recycling rate); best-available-tech (exhaust/waste-water treatment); **environmental-by-design** layout; early public/stakeholder dialogues.

Reputation/communications risk
Risk: Opacity on costs/timelines, misreading of transparency levels, or claims of "industry subsidy without return" can erode political support.
Mitigation: Strategic communications across all phases: quarterly milestones; public dashboard (trust KPIs, PDK releases, MPW slots); **show-and-tell** (open days, test-chip demos); crisis-comms playbook; lighthouse events (e.g., first **Trusted** label for a critical-infrastructure component).

Cross-cutting: "Comply-to-Connect" as a risk reducer
All clone fabs accept binding **baseline standards** (audit access, tool-family compliance, security, data classification) and may **opt into** additional co-operation modules (e.g., framework procurement, joint qualification runs) **without** exchanging commercially sensitive data. This enables scaling, keeps within competition law, and stabilises the quality of the **Trusted** label.

International context

The **Transparent Reference Fab (TRF)** is conceived as European infrastructure and remains **location-agnostic**. References to existing ecosystems (e.g., Switzerland, Spain, Ireland) serve solely for context, not as a country ranking. What matters is the **transferable blueprint**—tool families, open PDK, **Packaging-First**, **Comply-to-Connect**—that can be replicated at different European sites and in co-operation with partner countries.

Site decisions are taken project-by-project in **Phase 0** according to a transparent set of criteria (brownfield suitability, energy/utilities infrastructure, skills/academy, FDI/state-aid framework, security and audit requirements, packaging complementarity). This keeps the concept politically connectable, legally sound, and scalable—**without** implicit priority lists.

Conclusion and outlook

The **Transparent Reference Fab (TRF)** combines transparency, production readiness, and replicability to form a European infrastructure building block: **130 → 65 nm without EUV**, **Packaging-First** from day 1, an **open PDK**, and a **Comply-to-Connect** rulebook. The concept **complements** leading-edge initiatives rather than competing with them, addressing two core needs at once: additional, trustworthy manufacturing capacity and a replicable model that enables sites in Europe to scale quickly and with legal certainty.

Economically, a leverage effect arises with **moderate CAPEX corridors** (compared with <5-nm mega-projects), stabilised by **trusted-premium** (auditable provenance, long-term availability, quality KPIs) and **advanced-packaging** revenues (RDL/fan-out, interposer/2.5D, chiplets/UCIe). Network advantages are realised **voluntarily and in conformity with EU law** (open PDKs, joint MPWs/qualification runs, standardisation, procurement/data firewalls), steered via **blueprint/foundation governance**. The location

question is deliberately kept neutral: robust assessments are carried out only in **Phase 0** on the basis of transparent criteria, rather than generic country rankings.

Politically, the TRF requires **public infrastructure commitment**: a publicly accountable, European-embedded facility with a **public-trust mandate**, audit/security requirements, and **tranche-based financing** (FOAK/Chips Act/IPCEI + private capital). This ties risk, time, and funds to **milestones** (construction/tool IQ/OQ, open-PDK & MPW start, audit go-live, 65-nm release)—realistic within the window to **2030/31 (SOP 130 nm)** and **2031–33 (65-nm qualification)**, with explicit buffers.

Recommendation (starting signal):

1. **Set up an "Open Reference Fab" task force** (European Commission, Member States, industry, R&I); mandate: adopt a governance charter (Comply-to-Connect, tool-family policy, security/audit) within **90 days**.
2. **Launch Phase 0 (9–15 months):** brownfield screening, CAPEX/OPEX bottom-up, packaging scope, energy/utilities PPAs, workforce/academy plan, legal/state-aid pathway.
3. **Publish open-PDK seed & MPW schedule** (130-nm baseline, 65-nm roadmap), incl. a communications line: regular, audited disclosures of process/quality KPIs.
4. **Secure demand anchors:** LTAs (incl. take-or-pay), critical-infrastructure prioritisation, resilience retainers for automotive safety, aerospace/space-grade, energy/public transport.
5. **Fix tranching: Tranche 1** construction + base tools + MPW start (~40%); **Tranche 2** 65-nm ramp/tool upgrades (~35%); **Tranche 3** packaging pilot/co-packaging (~25%).

Closing statement: The Transparent Reference Fab is not a panacea—but it is a **scalable core element** of a European semiconductor strategy: it catalyses investment, closes value-creation gaps, binds talent, and strengthens security and trust. With a clear public mandate, lawful co-operation, and intelligent demand policy, a **replicable, durably competitive manufacturing ecosystem** emerges—**without permanent subsidies**. Europe thereby sends a clear message: we assume responsibility for our technological future—**transparent, collaborative, determined**.